REMARKS

Claims 1-23 as amended in the above list of claims are currently pending in the present patent application.

In Section 1 of the Office Action, the Examiner objects to Figure 1 for failing to include a suitable label such as "Prior Art." A replacement sheet for Figure 1 including the label "Background Art" accompanies this amendment. The Examiner also objects to the drawings in Section 2 of the Office Action for failing to show every feature of the invention specified in the claims. New drawings sheets containing new Figures 4-6 accompany this amendment such that the figures now illustrate all features recited in the claims. The new Figures 4-6 introduce no new matter into the application. The description of the depiction of the address generation methodology shown in Figures 4 and 5 is set forth in originally filed claims 3 and 4, for example. Figure 6 merely illustrates what was described in originally filed paragraphs 31-34 of the specification, for example. None of these new figures introduces any new matter into the application.

In Section 3 of the Office Action, the Examiner objects to the disclosure contained in the present specification and requests that the subject matter of the claims be placed in the specification. The paragraphs inserted after paragraph 38 in the above amendments to the specification ensure that every aspect of the present invention set forth in the currently pending claims is set forth in the specification. These paragraphs track the language of the claims and introduce no new matter into the application.

The Examiner rejects claims 3-4, 7-8, 14-15, and 18-19 in Sections 4 and 5 of the Office Action under the second paragraph of 35 U.S.C. § 112 for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. One skilled in the art will understand that the subject matter of the claims 3, 7 and 14 is fully supported by the description given in paragraph 31 of the specification. Similarly, one skilled in the art will understand that the subject matter of claims 4, 8, 15 and 19 is fully supported by the description given in paragraph 32 of the specification. These claims are directed, in part, to the implementations of an algorithm for generating the addresses for inputs for computing the butterfly operations.

A butterfly calculation requires three inputs: two data inputs and one twiddle factor. Claims 3-4, 7-8, 14-15, 18-19 are operations in an overall process or system corresponding to the calculations of the data input addresses, as will be understood by those skilled in the art. The paragraphs added following paragraph 32 in the Detailed Description and new Figures 4 and 5 merely present the subject matter recited in these claims in an alternative manner in an attempt to clarify this subject matter for the Examiner. These amendments to the specification and figures introduce no new matter into the application. The rejection of these claims under the second paragraph of Section 112 should accordingly be withdrawn.

In Sections and 6 and 7 of the Office Action to a Examiner rejects claims 1-23 under 35 U.S.C. § 101 as being directed to nonstatutory subject matter. The Examiner states that claims "1-23 cite a method and system for performing [an] FFT/IFFT in accordance with a mathematical algorithm." Claim 1 has been amended to recite a scalable method for implementing FFT/IFFT computations in multiprocessor architectures that provides improved throughput by eliminating the need for inter-processor communication after the computation of the first "$\log_2 P$" stages of the FFT/IFFT computations for a multiprocessor architecture including an implementation using "P" processing elements. Thus, the recited method is directed to a method of controlling calculations by processing elements in a multiprocessor system to perform desired FFT/IFFT computations. The method is not directed to the FFT/IFFT computations or algorithm itself. Such a method of controlling processing elements is a statutory process under Section 101. See claim 1 of U.S. Patent No. 5,293,330 to Sayegh (of record) as evidence of such a method corresponding to statutory subject matter.

Finally, in Sections 8 and 9 of the Office Action the Examiner rejects claims 1-2, 5-6, 9-10, and the 16-17, and 20-23 under 35 U.S.C. § 102(b) as being anticipated by the paper entitled "Performance Analysis of FFT Algorithms on Multiprocessor Systems" to Laxmi *et al.* ("Laxmi"). The Examiner rejects claims 11-13 under 35 U.S.C. § 103(a) as being obvious over Laxmi.

Amended claim 1 recites a scalable method for implementing FFT/IFFT computations in multiprocessor architectures that provides improved throughput by eliminating the need for inter-processor communication after the computation of the first "$\log_2 P$" stages of the FFT/IFFT computations for a multiprocessor architecture including an implementation using "P" processing elements. The method includes computing each butterfly of the first "$\log_2 P$" stages on either a single processing element or on each of the "P" processing elements simultaneously and distributing the computation of the butterflies in all the subsequent stages among the "P" processors such that each chain of cascaded butterflies consisting of those butterflies that have inputs and outputs connected together, are processed by the same processor.

With approach of Laxmi, the processing elements PE start to communicate with each other after $\log_2(N/P)$ stages. See page 513, right column, Section II, Radix-2 FFT Computation. Claim 1 expressly recites computing each butterfly of the first "$\log_2 P$" stages on either a single processing element or on each of the "P" processing elements simultaneously. Accordingly, according to this recited method communications among processing elements happens only after $\log_2 P$ stages. The computation of the butterflies are distributed in all the subsequent stages among the "P" processors such that each chain of cascaded butterflies consisting of those butterflies that have inputs and outputs connected together are processed by the same processor and thus such communication among processing elements occurs only once for the rest of the FFT computation. See the embodiment of the present invention depicted in Figures 2 and Figure 3. For large size FFTs the approach of Laxmi results in considerable interprocessor communication overhead.

For these reasons, the combination of elements recited in claim 1 is allowable. Dependent claims 2-4 are allowable for at least the same reasons as claim 1 and due to the additional limitations added by each of these dependent claims. With regard to claims 3 and 4, Laxmi neither discloses nor suggest generating addresses for the first and second operands and twiddle factor of a butterfly as recited in these claims. Claims 3 and 4 are therefore allowable for these additional reasons.

Amended claim 5 recites, in part a system for obtaining scalable implementation of FFT/IFFT computations in multiprocessor architectures that provides improved throughput by eliminating the need for inter-processor communication after the computation of the first "log2P" stages of the FFT/IFFT computations for a multiprocessor architecture including an implementation using "P" processing elements. The system includes a means for computing each butterfly of the first "log2P" stages on either a single processor or each of the "P" processors simultaneously. In Laxmi the processing elements PE start to communicate with each other after $\log_2(N/P)$ stages and not after $\log_2 P$ stages. The combination of elements in claim 5 is accordingly allowable and dependent claims 6-8 are allowable for at least the same reasons as claim 5 and due to the additional limitations added by each of these dependent claims.

Claim 9 recites, in part, a method of performing a fast Fourier transform or inverse fast Fourier transform on a plurality of inputs to generate a plurality of outputs, the method being performed on a plurality of processors and each transform including a plurality of stages containing at least one butterfly computational block. The method includes calculating the butterfly computational blocks for the first log2(P) stages of the transform on a single one of the processors or on a plurality of the processors operating in parallel. Once again, with Laxmi the processing elements PE start to communicate with each other after $\log_2(N/P)$ stages and not after $\log_2 P$ stages.

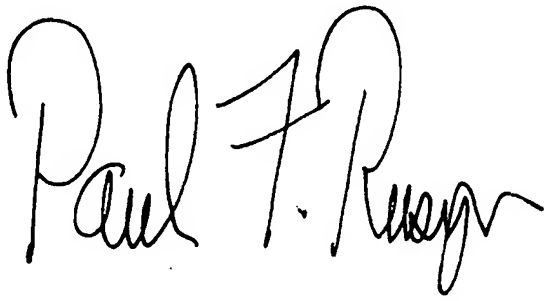
For the reasons, the combination of elements in claim 9 is allowable and dependent claims 10-15 are allowable for at least the same reasons as claim 9 and due to the additional limitations added by each of these dependent claims. Independent claims 16 and 21 are allowable for reasons similar to those just discussed with reference to claim 9. Claims that depend from claims 16 and 21 are allowable for at least the same reasons as the associated independent claim and due to the additional limitations added by each of these dependent claims.

The present patent application is in condition for allowance. Favorable consideration and a Notice of Allowance are respectfully requested. **If upon consideration of the present amendment the Examiner determines that any the pending claims are not in condition for allowance, the undersigned requests that**

the Examiner please contact him at (425) 455-5575 to discuss the outstanding issues. If any need for any fee in addition to that paid with this response is found, for any reason or at any point during the prosecution of this application, kindly consider this a petition therefore and charge any necessary fees to Deposit Account 07-1897.

Respectfully submitted,

GRAYBEAL JACKSON HALEY LLP



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